A Software Tool for PCIe® 4.0 Rx Lane Margining

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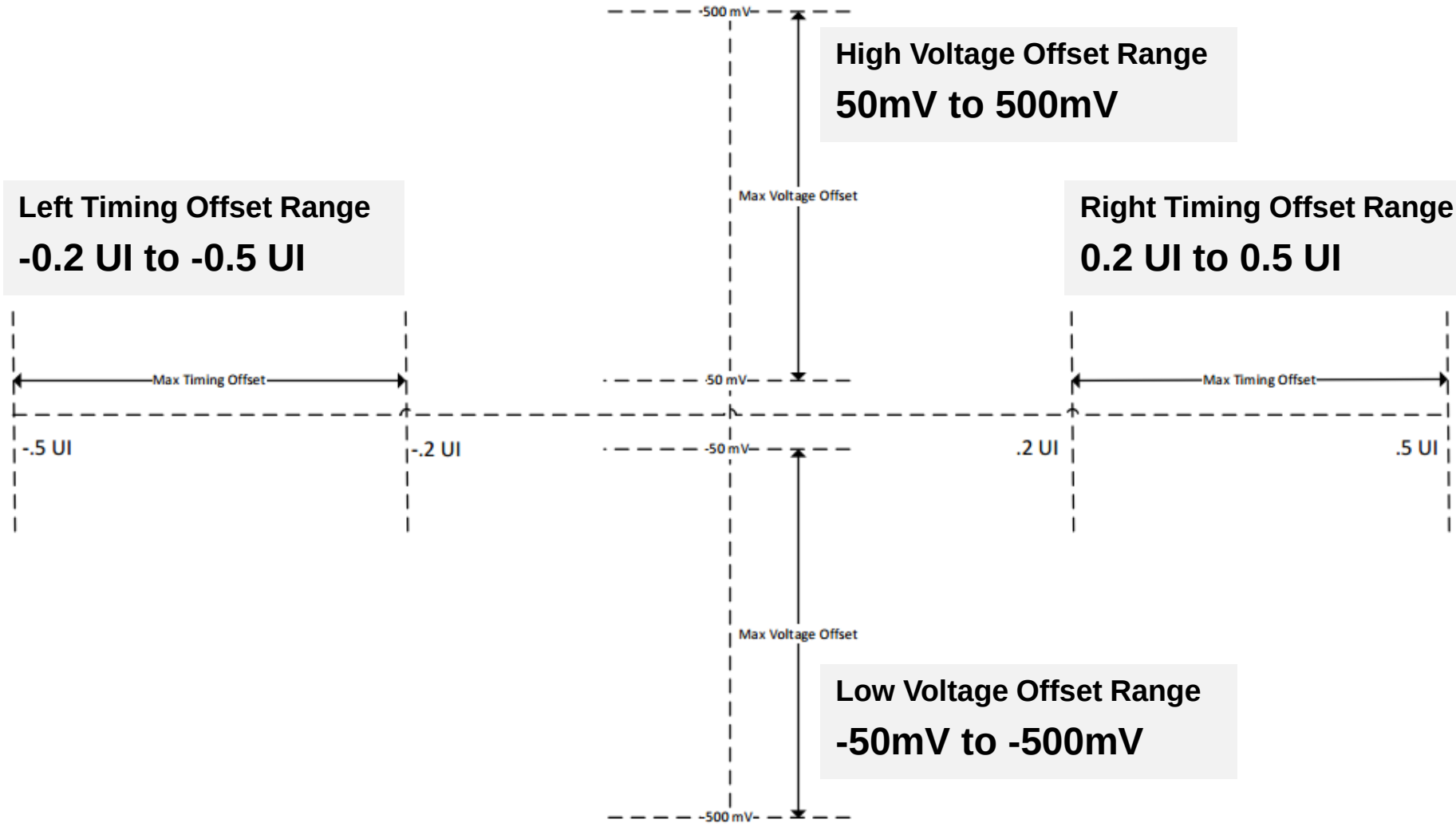
Outline

- **PCIe® 4.0 Rx Lane Margining**
- **PCIe 4.0 Rx Lane Margining Tool**
  - Features
  - Current Status
- **Example Margin Results**
- **Deployment Plans**

PCIe 4.0 Rx Lane Margining

- **New feature added to the PCIe 4.0 base spec**
- **Lane margining is mandatory for all ports that support 16 GT/s**
- **System SW obtains information for a given receiver while the Link is in L0**
- **Voltage margin (optional) and timing margin (mandatory)**
- **Independent timing margining is optional**

PCIe 4.0 Rx Lane Margining



High Voltage Offset Range

50mV to 500mV

Left Timing Offset Range

-0.2 UI to -0.5 UI

Right Timing Offset Range

0.2 UI to 0.5 UI

Low Voltage Offset Range

-50mV to -500mV

PCIe 4.0 Rx Lane Margining Tool

- **Intel is developing a receiver margining tool to be offered to the PCI-SIG for member use**
  - Developed using Python, source code to be provided
  - Can be used for a quick check of link segment electrical performance
  - Can identify poor performing lanes for detailed stress eye testing
- **The tool can margin the receivers on hosts, retimers, and endpoint devices**

Current Status

- **The tool is under development**
  - Supports root ports and endpoints
  - Command line based, GUI in development
- **Tool demo provided at the June 2017 PCI-SIG Developers Conference in Santa Clara at the Synopsys booth**
- **Successfully obtained margins with multiple PCIe 4.0 capable endpoint devices at the April and August 2017 PCI-SIG Compliance Workshops in Milpitas**

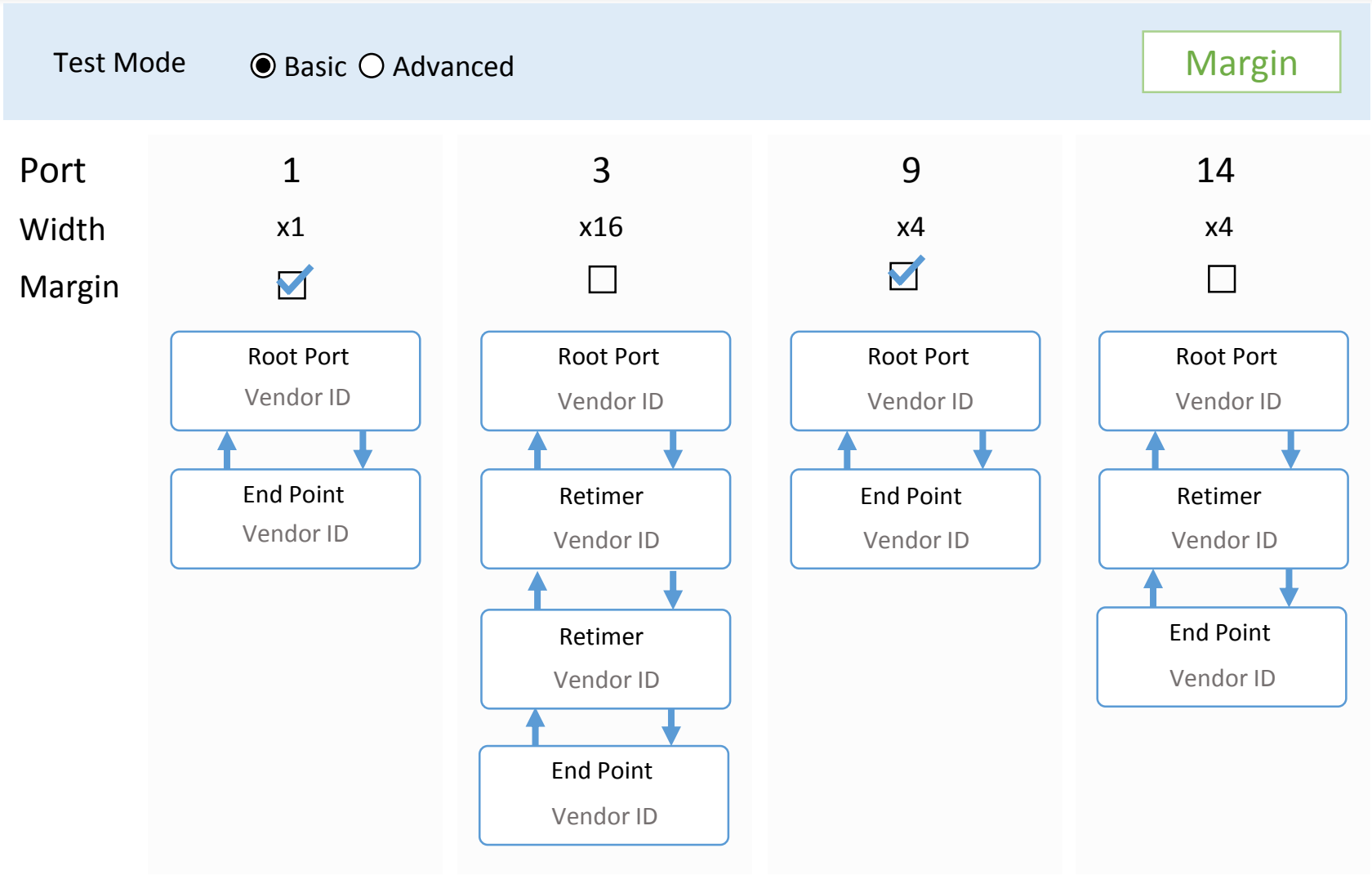
Features

- **Supports 2 different modes (Basic & Advanced)**
- **Basic Mode**
  - Margin all the receivers connected on the path
    - Margin upstream component (DSP)
    - Margin retimers (DSP and USP)
    - Margin downstream component (USP)
  - Port margining – All lanes to be margined
  - EW margining
  - EW margining per side – If implemented in silicon
  - EH margining – If implemented in silicon
  - Min dwell/BER per step using the spec minimum of 10^8

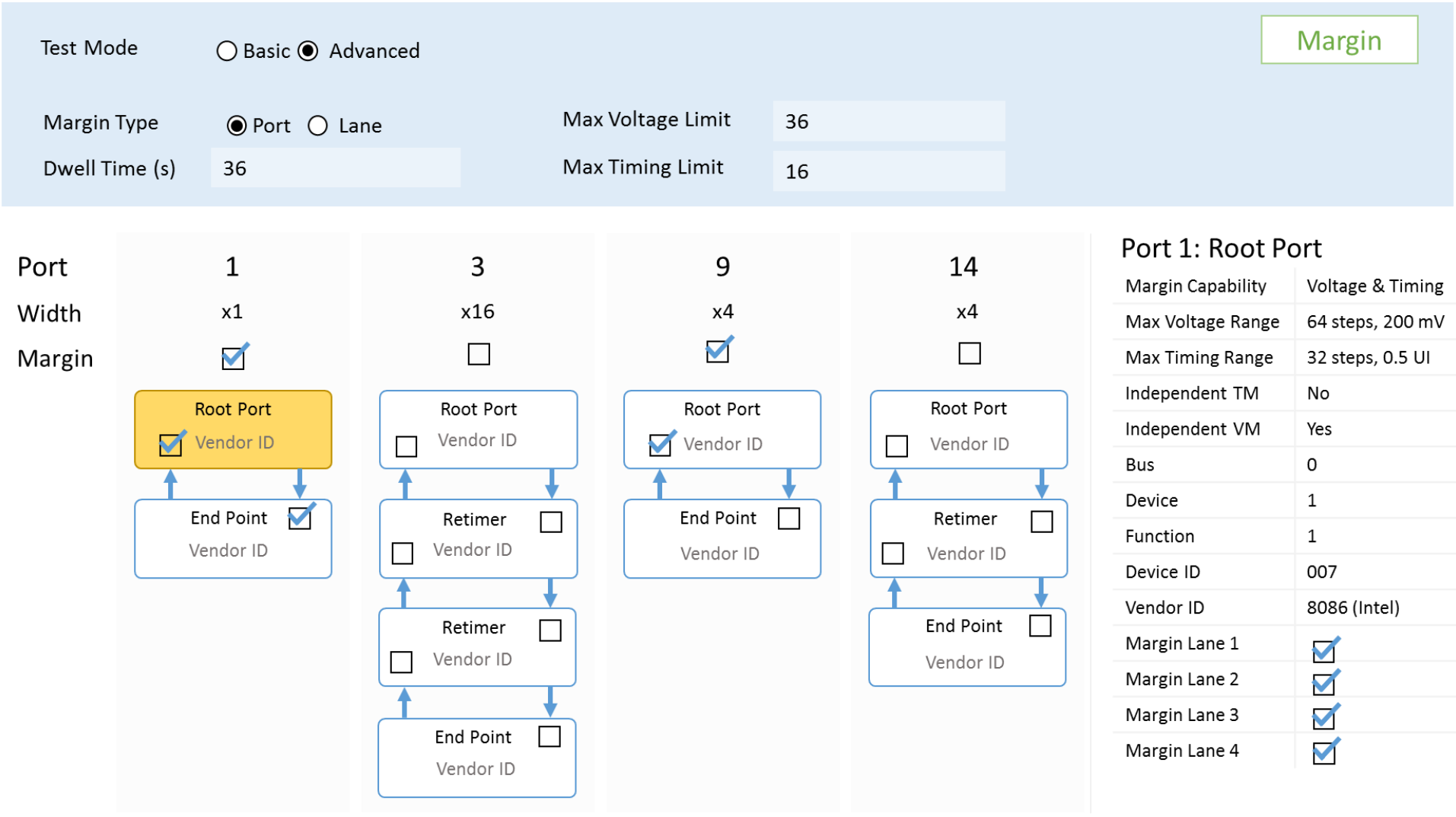
Features

- **Advanced Mode**
  - Per lane margining
  - Control error threshold
  - Control dwell/BER
  - 2 dwell time options for reduced test time
  - Target specific receivers
  - Set max range for EW and EH – In steps
- **Command line & GUI**
- **Plan to test with the following OS's**
  - Windows10
  - Linux

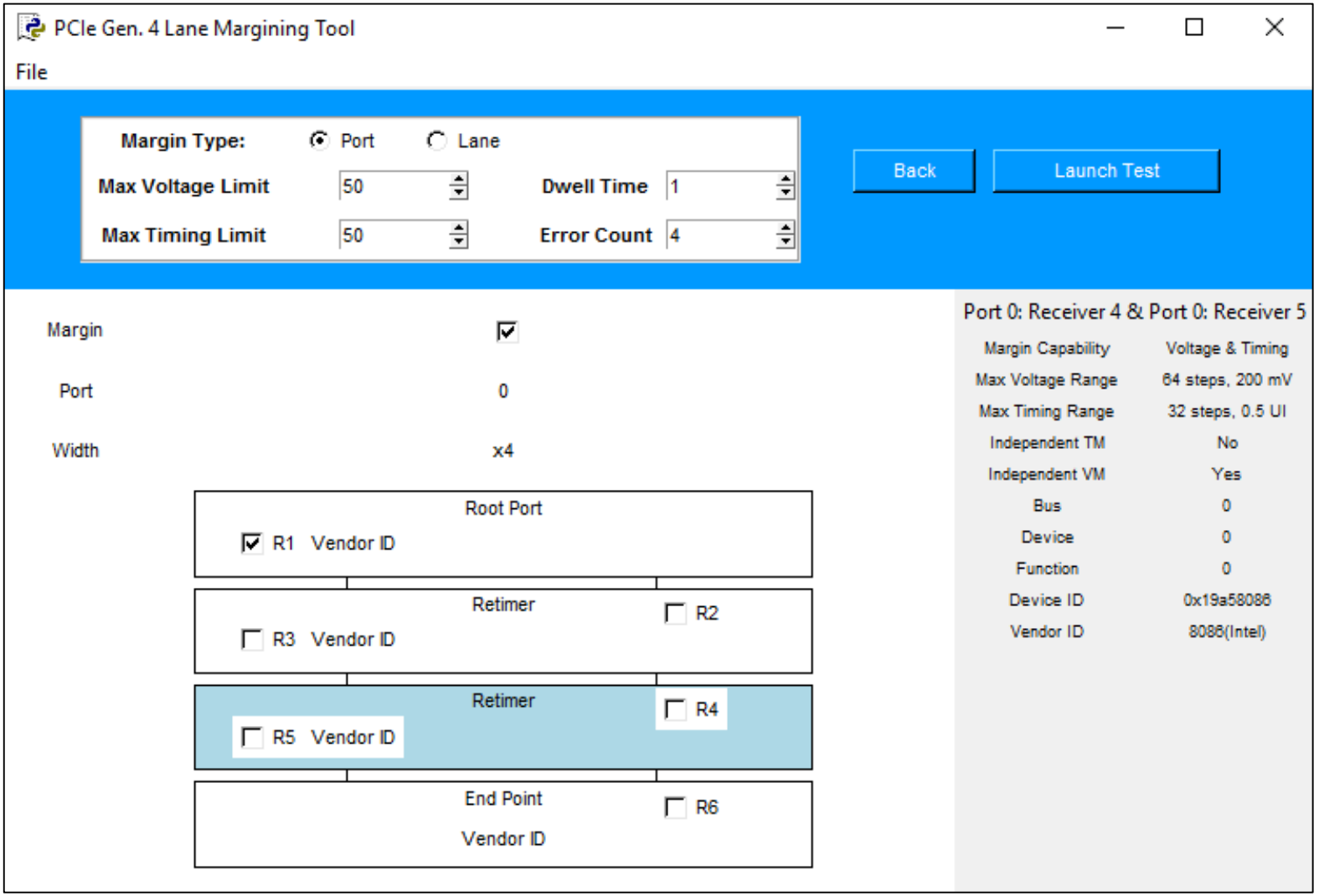
Basic Mode GUI Mockup



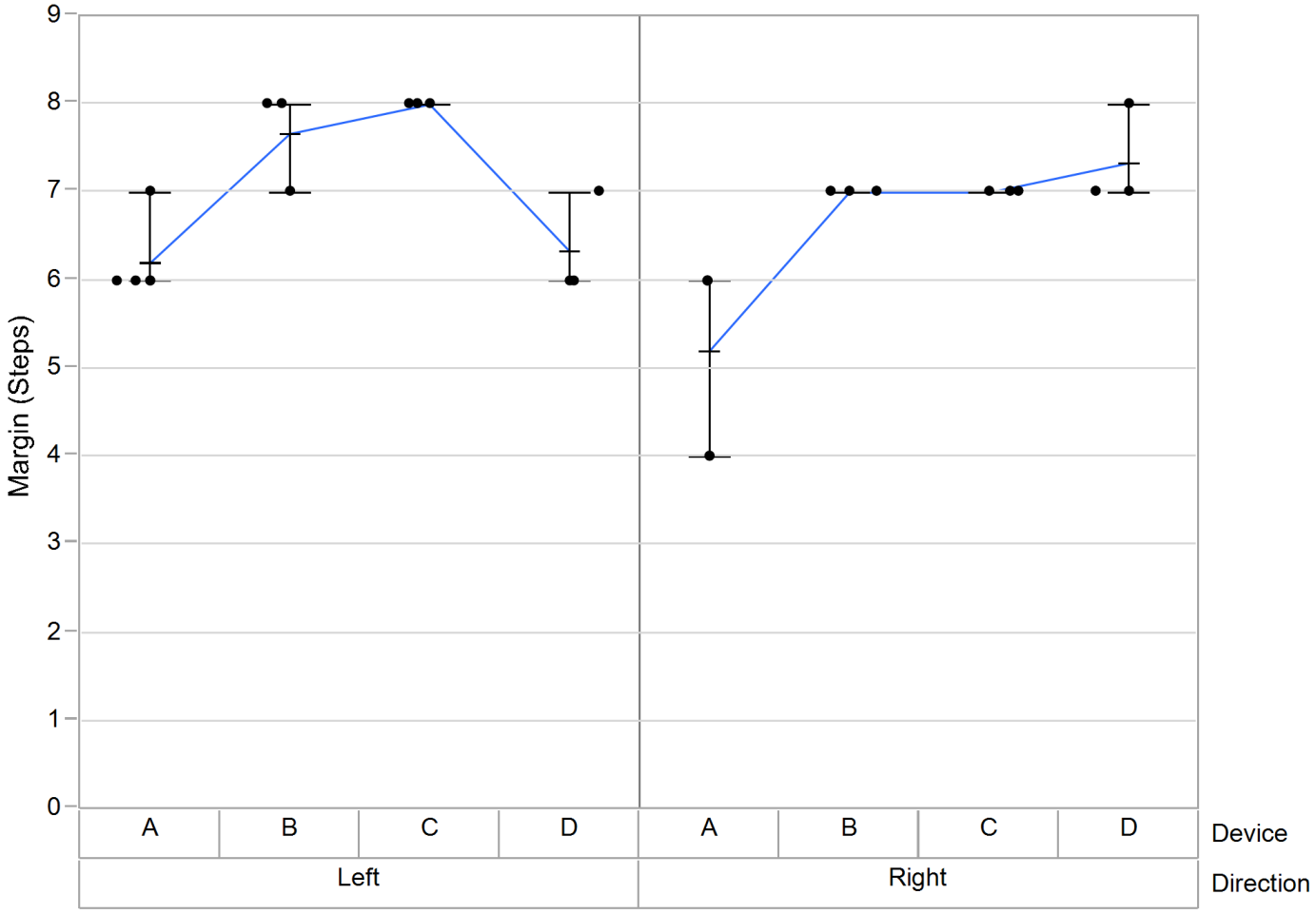
Advanced Mode GUI Mockup



Early GUI Prototype



Margining Example



Deployment Plans

- **Intel plans to provide the source to the PCI-SIG**
- **All decision on whether it will be accepted or released is up to the PCI-SIG**

Acknowledgements

The following individuals have contributed to the development of this tool

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For more information please go to www.pcisig.com